

Index

A

ASTAT	2-10, 2-13, 2-19, 2-24,
.....	2-26, 2-36, 3-21, 3-24, 12-5
Autobuffer service	5-39
Autobuffer timing	5-37
Autobuffering	5-3, 5-4, 5-26, 5-32, 5-38, 5-40,
.....	5-41, 8-1, 8-9, 8-10, 8-11, 8-12,
.....	8-13, 8-14, 8-15, 9-5, 9-23, 15-18
Autobuffer control register	5-27
AV (overflow) ...	2-2, 2-5, 2-8, 2-9, 2-13, 2-26, 2-36
AX0 register	2-5
AX1 register	2-5
AY0 register	2-5
AY1 register	2-5
AZ (zero)	2-5, 2-13

Bank select	3-23
Barrel shifter	1-6, 2-22
Base architecture	1-1, 1-6
BCR	9-13, 11-6, 11-7
BDMA	15-18
BDMA booting	9-13, 11-9
BDMA context reset	11-6, 11-7
BDMA interrupt	11-7
BEAD	11-4
BFORCE bit	10-16
BIAD	11-4
Binary multiplication	C-3
Binary string	2-1
Bit-reverse addressing	1-7, 3-23, 4-2, 4-6, 14-18
Block exponent	2-26
Block floating-point	1-5, 14-19, C-5
BMODE pin	7-3, 7-16, 10-15, 11-9, 11-12
<u>BMS</u>	1-8, 7-16, 10-17
Boot address	10-18
Boot loading	13-2, 13-5
Boot loading sequence	10-17
Boot loading through the HIP	7-16
Boot memory	10-1, 10-15, 10-17
Boot pages	10-15
Booting operation	9-4
BPAGE	10-16

Index

Branching	3-1
BTYPE	11-9
Buffer length	4-5
Bus exchange	1-5, 1-8, 2-15, 4-1, 4-9, 12-6
Bus grant (<u>BG</u>)	3-18, 9-15
Bus request (<u>BR</u>)	5-38, 10-15, 10-21, 13-2
Buses	1-3, 1-8
BWAIT	10-17
BWCOUNT	9-13, 11-7
Byte memory	11-9

C

C Compiler	1-10
C language	14-3
CALL	3-4, 3-8, 3-9, 3-24
Carry (AC)	2-2, 2-5, 2-8, 2-13, 2-36
Carry-in (CI)	2-5
Chip enable	10-3
Circular buffer addressing ...	1-5, 1-7, 4-1, 4-3, 4-8
CLKIN	9-1, 9-3, 9-4
CLKOUT	9-2, 9-3, 9-4, 10-2
Clock frequency	8-9
Clock signals	9-1
Clock synchronization (SPORT)	5-35
Clock synchronization delay (SPORT)	5-34
CNTR register	3-4, 3-9, 12-4
Codec interface	13-5
Companding	1-2, 5-5, 5-15, 5-23, 5-24, 5-25, 5-32, 5-36, 5-37, 5-42
Computation with data register move	15-7
Computation with memory read	15-6
Computation with memory write	15-6
Computational units	1-6, 3-23, 12-1, 12-6
Condition	3-20
Condition logic	3-3
Conditional instructions	3-24
Configuring interrupts	3-14
Context reset	11-7
Context switching	3-12
Continuous transmission	5-20
Control/status registers	1-12, E-1
Core architecture	1-5
Count stack	3-4, 3-5, 12-5
Counter expired (CE)	3-4, 3-6, 3-9
Cycle stealing	11-25

D

D/A	10-14
DAC	1-3
DAC interface	13-8
DAG1	1-7, 4-2, 12-2
DAG2	1-7, 3-3, 3-4, 3-8, 4-2, 12-2
Data address generators	4-1, 12-2
Data bus	4-1
Data memory	1-7, 1-8, 10-1
Data memory address bus	1-3, 1-8
Data memory data bus	1-3, 1-8
Data memory interface	10-10
Data memory read	15-6
Data structures	4-7
Data transfer	4-1
Denormalization	1-6
Denormalize	2-31
Derive block exponent	2-29
Derive exponent	2-22, 2-26
Development tools	14-2
Digital-to-analog conversion	13-5
Direct addressing	1-8
Divide primitives	2-9
Division exceptions	B-1
Division	2-9
DIVQ	2-10, 2-11, B-1
DIVS	2-2, 2-9, 2-10, B-1
DMA	15-18
DMA bus	1-8, 10-1
DMD bus	1-8, 2-19, 2-22, 3-4, 3-5, 3-20, 4-10, 10-1
DMD-PMD bus exchange	2-15, 4-1, 4-9, 4-10
DMOVLAY	10-31
<u>DMS</u>	1-8
DO UNTIL	3-4, 3-5, 3-6, 3-8, 3-9, 3-12, 12-5
DR input	5-2, 5-36
dreg	15-12, 15-14
DT output	5-2
Dual operand fetches	1-2, 1-5, 1-7

E

Edge-sensitive	3-15, 3-16, 3-18
Edge-sensitive interrupts	9-14
End-of-loop	3-7, 3-10
EPROM	1-4, 10-17

Index

EXP	2-33
EXPADJ	2-29
Exponent compare logic	2-22
Exponent detector	2-22, 2-26, 2-27
External address bus	1-3, 1-8
External clock	5-8, 9-21
External data bus	1-3, 1-8
External interrupts	9-14
External memory	5-38, 10-2
External SCLK	5-8
Extra cycles	15-18
EZ-ICE emulator	11-26

F

Fast fourier transform (FFT)	14-1, 14-11
Fast start-up	9-22
FIR filter	14-1, 14-4
Flag In (FI)	1-9, 3-24, 9-1
Flag Out (FO)	1-9, 9-1
Flag pins	9-15
Floating-point	2-33
Fractional mode	2-2, 2-3, 3-23, 3-24, C-1, C-4
Frame synchronization ..	5-2, 5-5, 5-10, 5-11, 5-12, 5-14, 5-15, 5-30, 5-34, 9-23
Framing	5-3, 5-16
Full duplex operation	5-34

G

GO mode3-23, 3-24, 5-38

H

HACK	7-3, 7-7, 7-9
Harvard architecture	1-2, 10-1
HDR overwrite mode	7-7, 7-9
HDR registers	7-4, 7-5, 7-6, 7-7
HI-extend (HIX)	2-26, 2-36
HI/LO reference signal	2-22, 2-24
HIP configuration modes	7-3
HIP data registers	3-15, 7-4, 7-5, 7-6, 7-7
HIP during powerdown	9-24
HIP interrupt	3-18, 7-9, 7-10, 7-11
HIP pin summary	7-2
HIP read interrupt	7-4
HIP status registers	7-6
HIP status synchronization	7-8
HIP timing	7-12, 7-13, 7-14, 7-15
HIP write interrupt	7-4
HMASK register	3-15, 7-4, 7-10, 7-11, 12-8

HMD0	7-3, 7-4
HMD1	7-4
Hold offs	11-25
Host	1-2
Host data bus	7-4
Host handshaking	7-7
Host interface port (HIP)	1-2, 1-9, 3-15, 7-1, 7-4, 9-4, 10-15, 12-2, 13-13
Host interface timing	7-11
Host read strobe	7-4
Host write strobe	7-4
HSEL	7-3
HSIZE	7-3, 7-11
HSR registers	7-4, 7-5, 9-25

I

I registers	4-2, 4-3, 5-26, 5-28, 8-14, 12-2
<u>IACK</u>	11-12, 11-13, 11-25
ICNTL register	3-14, 3-15, 3-16, 3-20, 9-14, 12-4
IDLE instruction.....	3-7, 3-10, 5-26, 9-15, 9-19, 9-26, 9-30
IDMA	11-12, 15-18
IDMA booting	11-24
IDMA control register	11-14, 11-15, 11-16
IDMA hold offs	11-25
IFC register	3-14, 3-18, 3-20, 12-4
IIR filter	14-1, 14-6
IMASK register	3-14, 3-15, 3-16, 3-19, 3-20, 7-10, 8-12, 9-14, 12-4
Immediate shifts	2-30
Indirect addressing	1-8, 4-3, 12-2
Indirect jumps	12-2
Input formats	2-18
Input registers	1-7
Instruction completion latencies	5-38, 15-18
Instruction set	15-1, A-1
Integer	3-23, 3-24, C-1
Integer mode	2-3, C-4
Internal buses	1-8
Internal memory	1-2
Internal oscillator	9-22
Interrupt control register	3-15
Interrupt controller	3-1, 3-3, 3-11
Interrupt force & clear register	3-15, 3-18
Interrupt latencies	3-19, 5-42
Interrupt mask register	3-16
Interrupt nesting	3-16
Interrupt request	5-40, 9-1, 9-14
Interrupt sensitivity	9-14

Index

Interrupt service 3-12, 3-14, 3-16,
..... 3-18, 3-20, 5-39
Interrupt vector 3-11, 3-12, 3-13,
..... 3-14, D-1, D-2, D-3
Interrupts 1-9, 3-4, 3-16, 9-24, 9-30, 12-4, 12-11
Interrupts pending 3-18
Interval timer 3-18, 3-23, 3-24
INVRFS 5-14, 5-16, 5-32
INVTDV 5-32
INVTFS 5-14, 5-16, 5-32
IRFS 5-11, 5-32
IRQ0 1-9, 3-11, 5-3, 9-14
IRQ1 1-9, 3-11, 5-3, 9-14
IRQ2 5-38, 9-14
ITFS 5-11

J

JUMP 3-8, 3-9, 3-24

L

Length (L) registers 4-1, 4-3, 4-4, 12-2
Level-sensitive interrupts 3-15, 9-14
Linker 14-3
Logical shift 2-3, 2-22, 2-28
Loop 3-5, 3-6, 3-7, 3-9
Loop comparator 3-3, 3-5, 3-6, 3-10
Loop counter 1-7, 3-4, 3-5, 12-4
Loop stack 3-4, 3-5, 3-6, 3-7, 3-22, 12-5
LSHIFT 2-31

M

M registers 4-1, 4-2, 4-3, 5-26, 5-28, 8-14, 12-2
MAC 1-6, 2-13, 2-15, 3-21,
..... 12-2, 12-6, 15-9, 15-10
MAC arithmetic 2-3
MAC input/output registers 2-18
MAC operations 2-16
MAC overflow 2-19
MAC saturation 2-19
Matrix multiply 14-1, 14-9
Memory address 3-3
Memory interface 10-2, 10-37, 12-2, 12-7
Memory read 10-3
Memory wait states 3-18
Memory write 10-3, 10-24
Memory-mapped registers 12-1
MF register 2-15, 2-20
Miscellaneous instructions 15-16
MMAP 7-16, 10-5, 10-6, 10-15
Mode bits 12-5

Mode control 12-5, 15-16
Mode status register (MSTAT) 3-12, 3-22
Modify (M) registers 4-1, 4-2, 4-3, 5-26, 5-28
Modulo addressing 4-1, 4-4
Modulus logic 4-3
MOVE instructions 15-13
MR register 2-13, 2-15, 2-16, 2-18, 2-20, 2-22
MR0 register 2-13, 2-15, 2-18
MR1 register 2-13, 2-15, 2-19, 2-20
MR2 register 2-13, 2-15, 2-19, 2-20
MSTAT 1-7, 2-8, 2-9, 2-16, 2-24, 3-12,
..... 3-14, 3-20, 3-22, 4-2, 6-1, 12-5
Multichannel 1-2, 1-8, 5-3, 5-5, 5-30
Multichannel frame delay 5-32
Multichannel length bit 5-31
Multichannel mode 5-30, 5-31, 5-32
Multichannel operation 5-32, 5-33
Multichannel setup 5-30
Multichannel transfer 5-32, 5-33
Multifunction instructions 1-4, 15-7, 15-19
Multiplication 2-13
Multiplier 2-18
Multiplier result format 2-17
Multiplier/accumulator 1-6, 2-13, 2-15, 3-21
Multiply/add 1-6
Multiply/subtract 1-6
Multiprecision capability 2-8
Multiprocessing 9-4
MV 2-13, 2-19
MX register file 2-15
MX0 register 2-15
MX1 register 2-15
MY register file 2-15
MY0 register 2-15
MY1 register 2-15

N

Nested loops 3-8
Nesting 3-15, 3-16
Next instruction address 3-3, 3-4, 3-7, 3-10
Normal framing mode 5-13
Normalize 2-22, 2-28, 2-33
Normalize modifiers 2-35
Numeric formats C-1

O

Off-chip memory accesses 15-18
On-chip memory 1-2
On-chip peripherals 1-2, 1-8
Opcodes A-1
Operating mode 3-22

Index

Operation during powerdown 9-23
 OR/PASS logic 2-22, 2-24
 Output enable 10-3, 10-24
 Output registers 1-7
 Overflow (AV)... 2-2, 2-5, 2-8, 2-9, 2-13, 2-26, 2-36
 Overwrite bit 9-24
 Overwrite mode 7-7, 7-9
 OWR CNTR 3-5

P

Page length 10-15, 10-18
 PASS 2-32, 2-33
 PC 3-4
 PC incrementer 3-3
 PC stack 3-3, 3-4, 3-6, 3-10, 3-11,
 3-22, 12-5, 15-84, 15-85
 PDFORCE 9-18
 Period register 6-1
 Periodic interrupts 6-1
 PMA bus 1-8, 3-3, 3-4, 3-8, 10-1, 10-3
 PMD bus 1-8, 10-1, 10-3
 PMD-DMD bus exchange... 1-5, 1-8, 2-15, 4-1, 4-9
 PMOVLAY 10-26
 PMS 1-8, 10-3, 10-24
 Polled operation 7-7
 PORT directive 10-14
 Powerdown 8-9, 9-17, 9-20, 9-30
 Powerdown acknowledge 9-29
 Powerdown control register 9-18, 9-20
 Powerdown force control bit 9-19
 Powerup 9-20
 Powerup boot 10-16
 Primary registers 2-7
 Processor states 9-2
 Program counter 3-4
 Program flow control 15-14, 15-15
 Program memory 1-8, 10-1
 Program memory configuration 10-5
 Program memory data bus 4-9
 Program memory interface 10-3
 Program memory map 10-5, 10-6
 Program memory read 10-3, 15-6
 Program memory write 10-3
 Program sequencer 3-1, 3-5, 12-2, 12-4
 Programming model 12-1
 PUCR 9-18
 PWAIT 10-5
 PWD pin 9-19
 PWDACK pin 9-29
 PX registers 1-5, 4-9, 4-10

Q

Quotient format 2-12

R

R bus 1-6, 2-15, 2-18, 2-22
 RAM 10-6
 Read operation 15-12
 Receive companding latency 5-40
 Receive frame sync 5-11, 5-12, 5-30
 Receive interrupt (SPORT) 5-4, 5-36
 Receive register 5-6
 Receive word enables 5-31
 Receiving data 5-6
 reg 15-12, 15-14
 Register indirect JUMPs 3-8
 Register notation 15-20
 Registers 12-1, 12-3
 RESET 9-1, 9-4, 9-21, 9-25
 Result bus 1-6
 Return 3-7, 3-10
 RFS 5-2, 5-11, 5-12, 5-30
 RFSDIV 5-12
 RFSDIV 12-7
 RFSR 5-10, 5-11
 RFSW 5-13
 Rounding mode 2-20
 RTI instruction 3-11, 9-15, 9-30
 RX register 5-2, 5-4, 5-32, 5-36
 RX0 register 5-6, 5-32
 RX1 register 5-6

S

Saturation 2-13
 SB register 2-22, 2-29
 SCLK 5-1, 5-12, 5-13, 5-15, 5-16
 SCLK frequencies 5-9
 SCLK pin 5-9
 SCLK0 5-34
 SCLK1 5-34
 SCLKDIV 5-9, 12-7
 SE register .. 2-22, 2-24, 2-26, 2-30, 2-31, 2-33, 2-34
 Secondary register 3-12
 Serial clock 5-1, 5-5, 5-8, 5-34, 5-38
 Serial clock frequencies 5-8
 Serial port autobuffering 5-42
 Serial ports 1-8, 5-1, 5-38, 9-5, 9-23, 12-7,
 13-5, 13-6, 13-7, 13-8, 13-10
 Serial word length 5-5, 5-9
 Shifter 1-6, 3-21, 12-2, 15-9, 15-11

Index

Shifter arithmetic 2-3
 Shifter array 2-22
 Shifter input/output registers 2-28
 Shifter operations 2-28
 Shifter sign 2-26
 SI register 2-22, 2-23
 Signed numbers 2-1
 Sine approximation 14-7
 SLEN 5-10, 5-16, 5-31, 5-32
 Software examples 14-1
 Software reboot 10-16
 SPORT 1-8, 3-18, 5-1, 5-3, 5-6, 9-23
 SPORT control register 5-8, 5-10, 5-11, 5-13,
 5-14, 5-16, 5-23, 5-31
 SPORT enable 5-7
 SPORT interrupts 5-3, 5-34, 5-41
 SPORT multichannel frame delay 5-31
 SPORT programming 5-4
 SPORT timing 5-34
 SPORT configuration 5-5
 SPORT0 5-1, 5-5, 5-15, 5-16, 5-30,
 8-13, 12-7, 13-6, 13-7
 SPORT0 configuration registers 5-5
 SPORT0 control register 5-30
 SPORT0 multichannel word enable registers 5-32
 SPORT1 5-5, 5-30, 8-9,
 8-13, 9-14, 9-15, 12-2
 SPORT1 alternate configuration 5-8
 SPORT1 configuration registers 5-5
 SR register 2-22, 2-23
 SR0 register 2-22, 2-24
 SR1 register 2-22, 2-24
 SSTAT 12-5
 Stacks 3-4, 12-5
 Start-up delay 9-20
 Start-up time 9-21
 Startup timing 5-38
 Status bits 3-21, 12-5
 Status condition 3-6, 3-25
 Status logic 3-4
 Status registers 3-15, 3-20
 Status stack 3-16, 3-20, 3-22, 12-5
 Stolen cycles 15-18
 Subroutine 3-9
 Subtract with borrow 2-8
 Synchronization delay 9-3
 Synchronization (serial clk to processor clk) ... 5-38
 System Builder 1-10
 System Control Register 9-14, 9-15,
 10-17, 15-12, E-1
 System interface 9-1

T

T1 interface 5-31
 TCOUNT 6-1, 6-2, 6-3, 6-4, 12-6
 TDV 5-32
 Termination condition 3-6, 3-10
 TFS 5-2, 5-11, 5-12, 5-30
 TFS0 5-30
 TFSR 5-10, 5-11
 TFSW 5-13
 Time-division multiplexed 5-30
 Timer 3-18, 3-23, 3-24, 6-1, 9-5, 12-2, 12-6
 Timer interrupt 3-19, 6-1
 Timer operation 6-3
 Timer registers 6-1, 6-2
 TOPPCSTACK 3-4, 3-25, 3-26, 3-27, 15-84, 15-85
 TPERIOD 6-1, 6-2, 6-3, 6-4, 12-6
 Transmit data valid 5-32
 Transmit frame sync 5-11, 5-12
 Transmit interrupt (SPORT) 5-4, 5-36
 Transmit register 5-6
 Transmit word enables 5-32
 Transmitting data 5-6
 TSCALE 6-1, 6-2, 6-3, 6-4, 12-6
 Twos-complement 2-1, 2-18, 2-33, C-1, C-4
 TX register 5-2, 5-4, 5-35
 TX0 register 5-6
 TX1 register 5-6

U

Underflows 2-8
 Unsigned 2-1, 2-18, C-1

W

Word length 5-3, 5-9, 5-32
 Write enable 10-3
 Write operation 15-12

X

XTAL pin 9-1, 9-21, 9-22
 XTALDELAY 9-18, 9-20
 XTALDIS 9-18

Z

Zero-overhead looping 1-5, 3-1